The office actions asserts that component 14 in Figure 2 of Tavallaei corresponds to the recited scaleable node controllers. However, Tavallaei describes component 14 as a local advanced programmable interrupt controller (APIC). A local APIC is not identical to a scaleable node controller.

The office action asserts that component 26 in Figure 2 of Tavallaei corresponds to the recited scalability port switch. However, Tavallaei describes component 26 as an external input / output advanced programmable interrupt controller (I/O APIC). An I/O APIC is not identical to a scalability port switch.

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Tavallaei fails to teach or suggest this further recitation. In contrast to the present invention, Tavallaei describes a multi-processor system with local APICs 14 connected to the I/O APIC 26 over the APIC bus 16. Tavallaei describes that the I/O APIC 26 generates an interrupt message on the APIC bus 16, which is monitored by all the local APICs 14. The local APICs 14 appear to be responsive to the content of the interrupt messages for passing on local interrupts for the associated processor 12. The Examiner has not identified (and applicants are unable to identify) any portion of Tavallaei that teaches or suggests that the local APICs 14 have addresses associated therewith.

Because Tavallaei fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Tavallaei, and is patentable over Tavallaei. Claims 2-3 depend from claim 1 and are likewise patentable.

With respect to claims 9 and 18, for the reasons given above Tavallaei does not disclose the recited scaleable node controller or the recited scalability port switch. Moreover, Tavallaei does not determine which local APIC 14 receives the interrupt request. Rather, Tavallaei generates an interrupt message on the APIC bus 16 which is monitored by all the local APICs 14. Accordingly, claim 9 and its dependent claims 10-12 and 16-17 are not anticipated by and are patentable over Tavallaei. Likewise, claim 18 and its dependent claims 19-21 and 25-26 are patentable over Tavallaei.

With respect to claims 11 and 20, the office action identifies col. 7 lines 41-44 for the recited comparing a priority of the interrupt request with a priority of the processor.

However, the cited portion makes no reference whatsoever to a priority of the processor. Accordingly, claims 11 and 20 are separately patentable over Tavallaei.

Claims 1-3, 9-12, 14-21, and 23-26 are rejected under 53 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,944,809 (Olarig). Applicants respectfully traverse this rejection for the following reasons.

In order to anticipate, the reference must identically disclose each claim element. In fact, Olarig does not identically disclose many of the recited claim elements.

The office actions asserts that components 107 and 306 in Figure 4 of Olarig corresponds to the recited scaleable node controllers. However, Olarig describes component 107 as a cache and component 306 as a local programmable interrupt controller (LOPIC). A cache and a LOPIC is not identical to a scaleable node controller.

The office action asserts that component 312 in Figure 4 of Olarig corresponds to the recited scalability port switch. However, Olarig describes component 312 as a central programmable interrupt controller (COPIC). A COPIC is not identical to a scalability port switch.

Among other things, claim 1 further recites that the scalability port switch is to determine an address of one of said scaleable node controllers from said interrupt request. Olarig fails to teach or suggest this further recitation. In contrast to the present invention, Olarig describes a multi-processor system with LOPICs 306 connected to the COPIC 312 over the PIC bus 311. Olarig appears to function similarly to Tavallaei as discussed above. The Examiner has not identified (and applicants are unable to identify) any portion of Olarig that teaches or suggests that the LOPICs 306 have addresses associated therewith.

Because Olarig fails to teach or suggest any of the recited scaleable node controller, scalability port switch, or an address for the scaleable node controller, claim 1 is not anticipated by Olarig, and is patentable over Olarig. Claims 2-3 depend from claim 1 and are likewise patentable.

With respect to claims 9 and 18, for the reasons given above Olarig does not disclose the recited scaleable node controller or the recited scalability port switch. Accordingly, claim 9 and its dependent claims 10-12 and 14-17 are not anticipated by and are patentable

over Olarig. Likewise, claim 18 and its dependent claims 19-21 and 23-26 are patentable over Olarig.

With respect to claims 11 and 20, the office action identifies col. 10. lines 8-10 for the recited comparing a priority of the interrupt request with a priority of the processor. However, the cited portion makes no reference whatsoever to a priority of the interrupt request. Accordingly, claims 11 and 20 are separately patentable over Olarig.

Claims 4 and 5 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,119,191 (Neal). Applicants respectfully traverse this rejection for the following reasons.

Neal fails to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness.

Moreover, claim 4 recites a first input/output hub coupled between the peripheral component interconnect bus and the first scalability port switch, wherein said first input/output hub is able to support a plurality of additional peripheral component interconnect hubs. The office action asserts that component 28 corresponds to the recited hub. However, component 28 is simply described as an ASIC connected to a PCI bus, not an I/O hub. In fact, the word "hub" cannot be found in Tavallaei. No one skilled in the art would be motivated to replace the ASIC 28 of Tavallaei with the hubs described in Neal.

Because the office action fails to establish a prima facie case of obviousness and because the ASC 28 is not an I/O hub, claim 4 is patentable over Tavallaei in view of Neal. Claim 5 depends from claim 4 and is likewise patentable.

Claims 6 and 7 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, and further in view of Olarig. Applicants respectfully traverse this rejection for the following reasons.

Neal and Olarig both fail to make up for the above-noted deficiencies in Tavallaei. Accordingly, the office fails to establish a prima facie case of obviousness. Claim 6 and 7 depend from claim 5, and are accordingly patentable for the reasons given above. Claims 6 and 7 are further patentable for the following reasons.

Claim 6 recites that the first pair of scaleable node controllers and the second pair of scaleable node controllers are coupled to a second scalability port switch. Claim 7 depends from claim 6 and further recites that the second scalability port switch is coupled to the first input/output hub. Each of Tavallaei and Olarig describe that the respective local APICs 14 and the LOPICs 306 are closely associated with a single processors, identifying and handling interrupts for only the closely associated processor. Olarig does not suggest the type of interconnectivity recited in the claims. The multiple COPICS mentioned in Olarig appear to relate to a hierarchically distributed interrupt handling arrangement, and not to any LOPIC being coupled to more than one COPIC.

Because the office fails to establish a prima facie case of obviousness and because Olarig does not teach or suggest two pair of scaleable node controllers with each pair connected to two different scalabilit port switches, claims 6 and 7 are separately patentable over Tavallaei in view of Neal and further in view of Olarig.

Claim 8 is rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei, in view of Neal, further in view of Olarig, and further in view of U.S. Patent No. 6,606,676 (Deshpande). Applicants respectfully traverse this rejection for the following reasons.

None of the secondary references make up for the missing teachings of Tavallaei noted above. For example, none of the cited references even mentions a scalability port switch. Therefore, the office action fails to establish a prima facie case of obviousness. Moreover, the office action fails to provide legally sufficient motivation to combine or modify the references in the manner suggested. The office action appears to use the claims as a blueprint to pick and choose pieces of prior art which allegedly read on various claim recitations without identifying any portion of the references which actually suggests the desirability of any of the proposed modifications. In particular, no one skilled in the art would be motivated to combine the multiplicity of references as applied in the rejection of claim 8, absent the teachings of the present application.

In particular, the office action suggests modifying Tavallaei to have multiple processors connected to the local APIC 14. This is simply unworkable. The local APICs are dedicated to the local processors 12, which Tavallaei describes as preferably being located on

the same chip (see col. 6, lines 9-13). No one skilled in the art would be motivated to modify Tavallaei in the manner proposed in the office action.

The office action asserts that the combination of four references is obvious "because it would reduce traffic on the bus shared between the nodes." However, this motivation is completely contrived and without basis or citation to any of the references. If the rejection is maintained, applicants respectfully request that the Examiner identify every element of Tavallaei which is proposed to be modified and the textual or other basis which suggests making such modification.

Because the secondary references fail to make up for the deficiencies in Tavallaei, and because there is no motivation to combine the references as suggested by the office action, claim 8 is separately patentable over the cited combination of references.

Claims 13 and 22 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Tavallaei in view of U.S. Patent No. 6,189,065 (Arndt). Claims 13 and 22 are also rejected under 35 U.S.C. § 103(a) as being unpatentable over Olarig in view of Arndt. Applicants respectfully traverse these rejections for the following reasons.

Arndt fails to make up for the above noted deficiencies in Tavallaei and Olarig. Accordingly, the office action fails to establish a prima facie case of obviousness.

The office action fails to address several of the claim recitations. For example, each of claims 13 and 22 recite that the scaleable node controller redirects the interrupt request. The cited portion of Arndt describes offloading an interrupt request, but does not teach or suggest that a local APIC or LOPIC should be modified to perform such offloading. Each of claims 13 and 22 further recite that the interrupt request is redirected through the scalability port switch. Again, the cited portion of Arndt is silent in this regard.

Moreover, the local APIC of Tavallaei and the LOPIC of Olarig are tightly coupled with their respective associated processors, identifying and handling interrupts for those processors. Again, for the purpose of emphasis, the local APICs and LOPICs of these references are simply not scaleable node controllers. One of ordinary skill in the art would not be motivated be modify a local APIC or a LOPIC to perform such higher level interrupt distribution, such as redirecting interrupt requests.

Because the Arndt fails to make up for the respective deficiencies in Tavallaei and Olarig, and because there is no motivation to combine the references as suggested by the office action, claims 13 and 22 are separately patentable over the cited combination of references.

In view of the foregoing, favorable reconsideration and withdrawal of the rejections is respectfully requested. Early notification of the same is earnestly solicited. If there are any questions regarding the present application, the Examiner is invited to contact the undersigned attorney at the telephone number listed below.

Respectfully submitted,

August 27, 2004
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CERTIFICATE OF TRANSMISSION

I hereby certify that this correspondence is being facsimile transmitted to the U.S. Patent and Trademark Office on the date shown below.

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